IN THE CLAIMS

Please cancel claims 4-7 without prejudice or disclaimer.

Claim 1 (currently amended) A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at least one component including a polysilicon layer having a top surface, wherein the at least one component is formed on a field oxide region configured to separate the plurality of gate stacks;

a silicide on the top surface of the polysilicon layer of the at least one component; and

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein.[, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and

a conductor for filling the plurality of contact holes;

wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.]

Claim 2 (original) The flash memory device of claim 1 wherein the silicide further includes a titanium silicide.

Claim 3 (original) The flash memory device of claim 1 wherein the silicide further includes a cobalt silicide.

Claims 4-7 (cancelled)

Claims 8-16 (withdrawn)

Claim 17 (new) A flash memory device, comprising:

an oxide layer;

a gate stack formed on said oxide layer, wherein said gate stack comprises:

a first polysilicon layer;

an insulating layer formed on said first polysilicon layer; and

a second polysilicon layer formed on said insulating layer;

a field oxide region located adjacent to said oxide layer;

a component located on said field oxide region, wherein said component is formed from one of said first and said second polysilicon layer; and

a silicide layer formed on said component.

Claim 18 (new) The flash memory device as recited in claim 17, wherein said silicide layer on said component prevents etching through one of said first and said second polysilicon layer.

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Claim 19 (new) The flash memory device as recited in claim 17, wherein said silicide layer comprises a titanium silicide.

Cont

Claim 20 (new) The flash memory device as recited in claim 17, wherein said silicide layer comprises a cobalt silicide.

Claim 21 (new) The flash memory device as recited in claim 17, wherein said component comprises a resistor.